P-Channel 30V (D-S) MOSFET

GENERAL DESCRIPTION

The 3401A is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦68mΩ@V_{GS}=-10V
- $R_{DS(ON)}$ ≦80mΩ@V_{GS}=-4.5V
- $R_{DS(ON)}$ ≦100mΩ@V_{GS}=-2.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

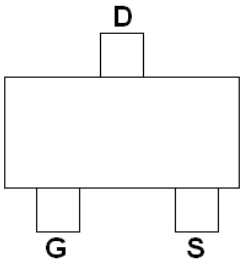
APPLICATIONS

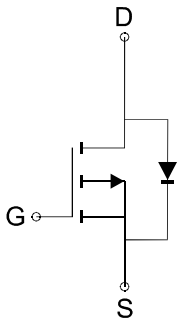
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION

(SOT23-3L)

Top View





P-Channel MOSFET

Ordering Information: 3401A (Pb-free)

Absolute Maximum Ratings (T_A=25℃)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A=25	I_D	-4.2	A
	T_A=70℃		-3.5	
Pulsed Drain Current		I_{DM}	-14	A
Maximum Power Dissipation	T_A=25℃	P_D	1.4	W
	T_A=70℃		0.9	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	90	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

P-Channel 30V (D-S) MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

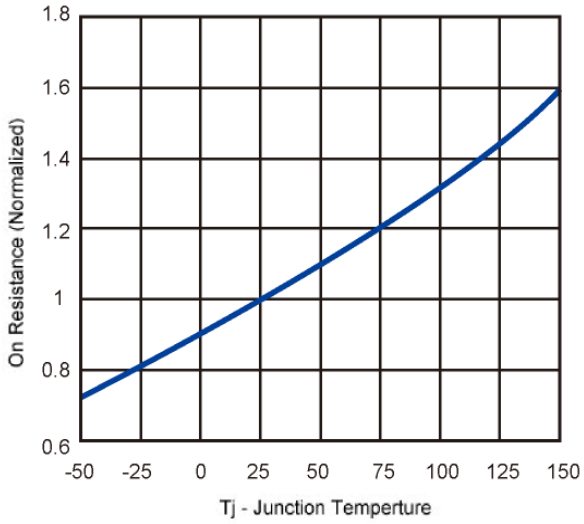
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-0.6		-1.3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D= -4.2A		57	68	mΩ
		V_{GS}=-4.5V, I_D= -4A		62	80	
		V_{GS}=-2.5V, I_D= -2A		80	100	
V_{SD}	Diode Forward Voltage	I_S=-1A, V_{GS}=0V		-0.7	-1	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=-15V, V_{GS}=-4.5V, I_D=-4A		9		nC
Qgs	Gate-Source Charge			2.3		
Qgd	Gate-Drain Charge			2		
Ciss	Input Capacitance	V_{DS}=-15V, V_{GS}=0V,f=1MHz		710		pF
Coss	Output Capacitance			70		
Crss	Reverse Transfer Capacitance			20		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-15V, R_L =3.6Ω R_{GEN}=6Ω, V_{GS}=-10V		37		ns
t_r	Turn-On Rise Time			23		
$t_{d(off)}$	Turn-Off Delay Time			46		
t_f	Turn-Off Fall time			3		

Notes: pulse width ≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

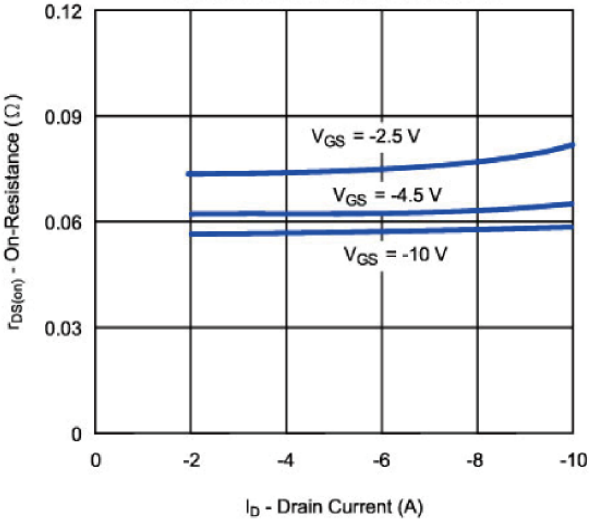
P-Channel 30V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

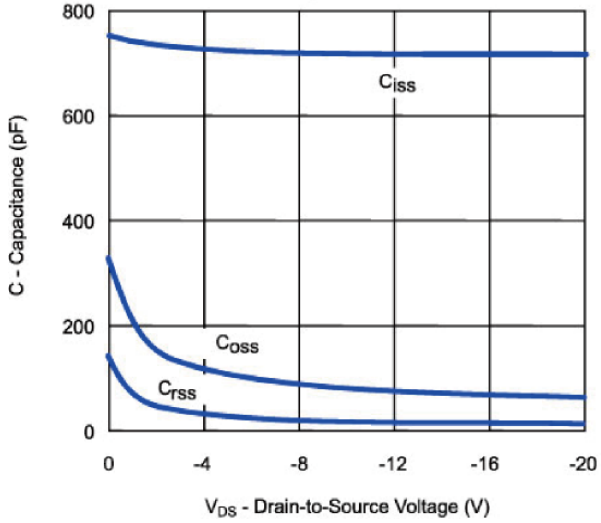
On Resistance vs. Junction Temperture



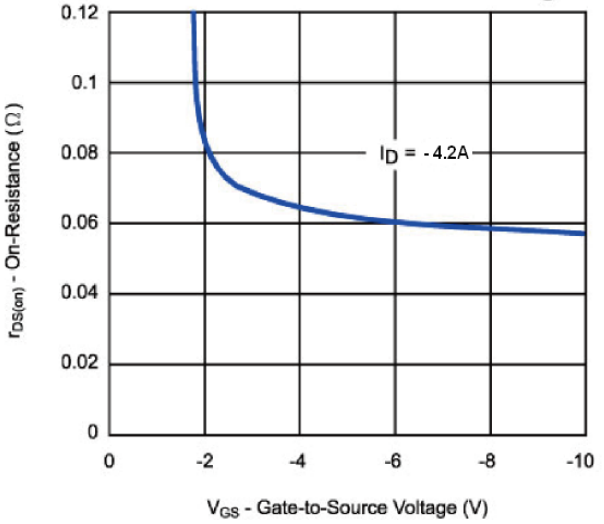
On-Resistance vs. Drain Current



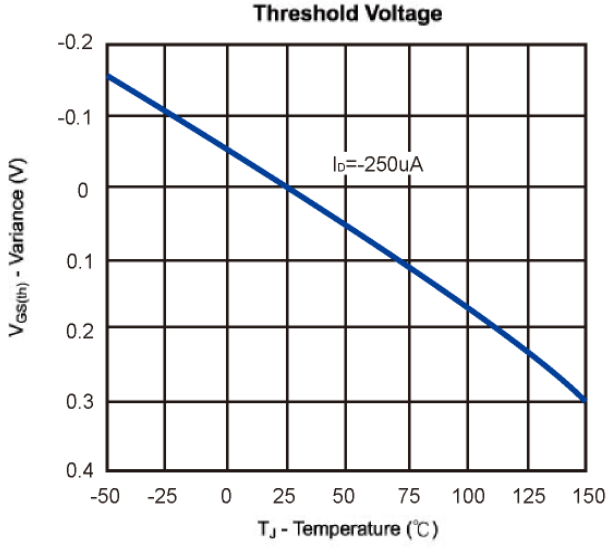
Capacitance



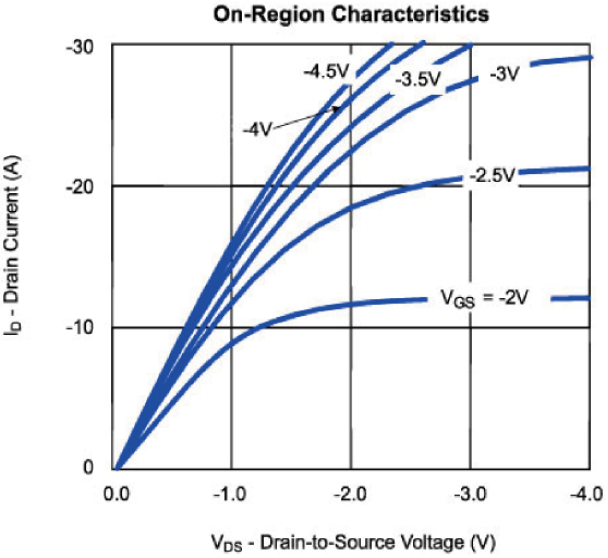
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



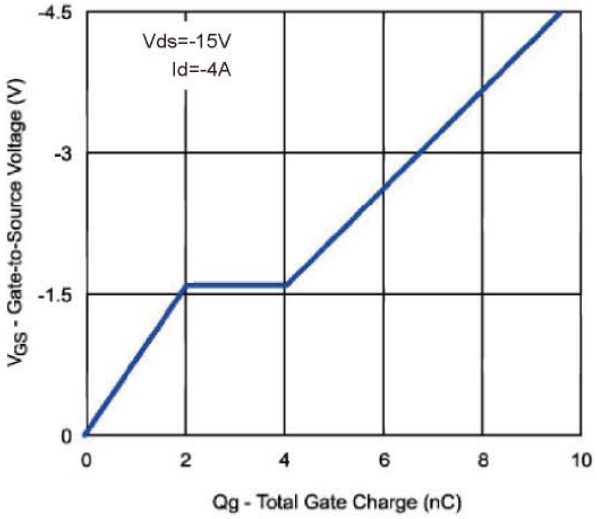
On-Region Characteristics



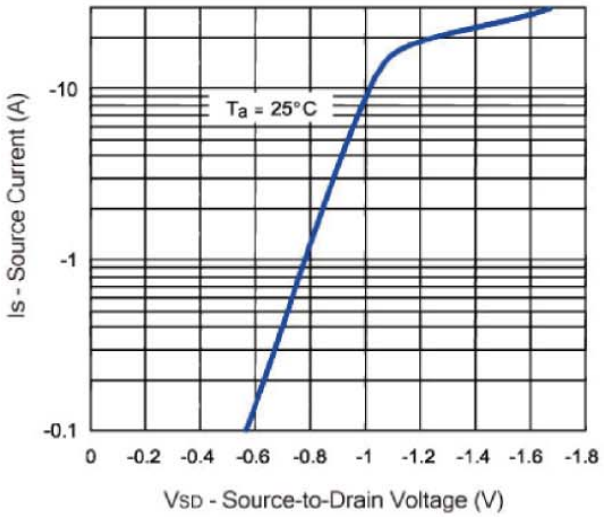
P-Channel 30V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

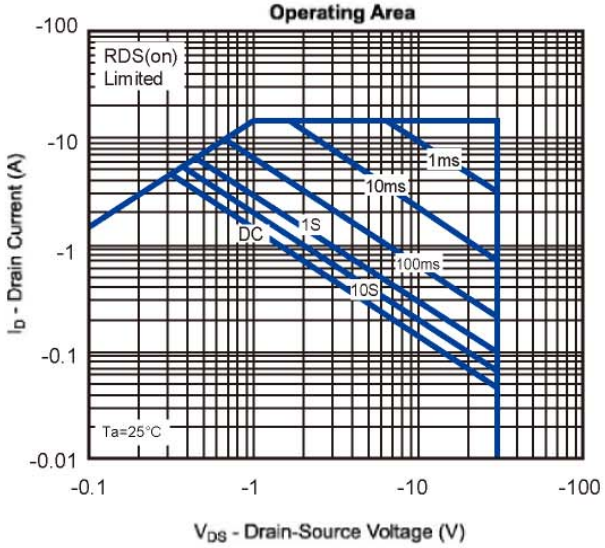
Gate Charge



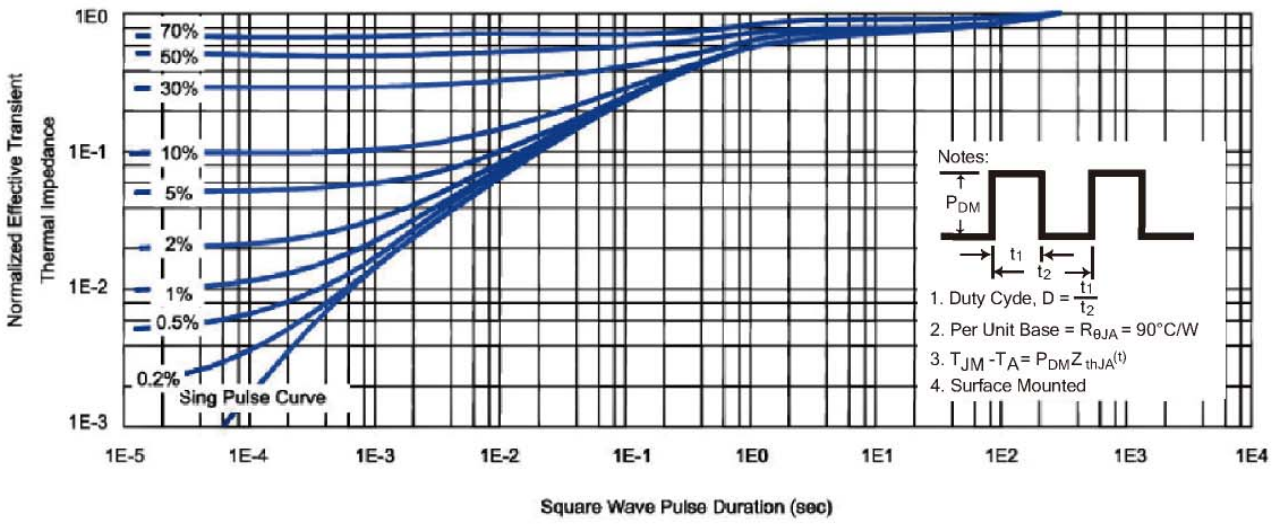
Body-diode characteristics



Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



P-Channel 30V (D-S) MOSFET

SOT23-3L Package Outline